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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,092	06/27/2001	Kazutaka Shibata	ROH-037	1091

7590 12/28/2005

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EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1722	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/830,092	SHIBATA, KAZUTAKA	
	Examiner	Art Unit	
	Matthew J. Song	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,6,17-20 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-20 and 29* is/are allowed.

6)☒ Claim(s) *3, 4, 6, and 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/11/2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 4, 6, 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (WO99/09595), where US 6,495,914 is used as an accurate translation and an accurate translation can be provided upon request, in view of Fukasawa et al (US 6,455,920) and Ichikawa (JP 02-031437), where an English Abstract has been provided and an accurate translation can be provided upon request.

Sekine et al discloses all of the limitations of claim 3, as discussed previously, except a step for forming a back side resin layer on a back side of the semiconductor substrate and removing a back side resin through polishing or grinding from the semiconductor substrate.

In a method of forming a semiconductor device, Fukasawa et al teaches a semiconductor device **20A** with a resin layer **41** provided on the rear surface of the semiconductor chip. Fukasawa et al teaches the semiconductor chip is improved and problem damages in the bottom surface of the chip at the time of dicing the semiconductor wafer **51** into individual chips is eliminated (col 17, ln 35 to col 18, ln 67 and Figs 23-26). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify to modify Sekine et al with Fukasawa et al's resin layer on the bottom of the chip to eliminate damage to the bottom of the semiconductor chip during dicing.

The combination of Sekine et al and Fukasawa et al does not teach a back side grinding step of thinning the semiconductor substrate by removing the back side resin through polishing or grinding, from the semiconductor substrate.

In a method of packing a semiconductor chip, Ichikawa teaches a semiconductor chip is sealed in resin **21** and the rear side of the chip is subjected to grinding for a reduction in the packaging height. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify to modify the combination of Sekine et al and Fukasawa et al with Ichikawa's grinding of a resin layer to reduce the height and enhance the packaging density.

Referring to claim 3, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches a step of forming a surface resin layer **48** ('914), a back side resin layer **41** ('920) and a back side grinding step ('437) and further polishing the back side of the semiconductor ('914 col

6, ln 35-40). It is also noted that further polishing is not patentable because splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result was held to be not patentably distinguish the processes (Ex Parte Rubin 128 USPQ 159). The combination of Sekine et al, Fukasawa et al and Ichikawa teaches forming projections **43** ('914). The combination of Sekine et al, Fukasawa et al and Ichikawa teaches grinding or polishing ('914 col 6, ln 20-30).

The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the order of processing steps. The transposition of process steps where the processes are substantially identical or equivalent in terms of function, manner and result was held to be not patentably distinguish the processes ((Ex Parte Rubin 128 USPQ 159) and MPEP 2144.04).

The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the surface resin and the backside resin are substantially the same thickness. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by optimizing the thickness of the resin layer by conducting routine experimentation to obtain same.

The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to bracing the substrate with the back side resin layer while the performing the surface grinding step so as to inhibit warpage of the substrate. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa to perform the surface grinding step first; therefore the bracing the substrate with the backside resin layer would habe naturally flowed from the suggestion of the prior art. The fact that applicant has recognized another advantage which would flow naturally from following the

suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Referring to claim 4, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches cutting the substrate after grinding ('914, col 6, ln 30-45).

Referring to claim 6, the combination of Sekine et al, Fukasawa et al and Ichikawa teahes the projections are embedded in the resin layer ('914 col 6, ln 5-40 and Figs 4a-4d).

Referring to claim 26, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches cutting along the centers between the adjacent shield walls after grinding ('914 col 8, ln 40-60), this reads on applicant's cutting along cutting lines after completing the back side grinding step. The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to polishing or grinding the surface resin layer such that the remaining surface layer has a thickness that is uniform. Uniformity is well known in the semiconductor art to be required to increase yield, which is desirable. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by polishing or grinding the surface resin layer such that the remaining surface layer has a thickness that is uniform because increased uniformity is desirable in semiconductor manufacturing to increase yield.

Referring to claims 27 and 28, the combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the surface resin layer is formed with uniform thickness and grinding the surface resin layer so that the heights of the plurality of projection electrodes is uniform. Uniformity is well known in the semiconductor art to be required to increase yield, which is desirable. It would have been obvious to a person of ordinary skill in the art at the time of the

invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by forming a surface resin layer with uniform thickness and grinding the surface resin layer so that the heights of the plurality of projection electrodes is uniform because increased uniformity is desirable in semiconductor manufacturing to increase yield.

Response to Arguments

4. Applicant's arguments, see page 6 of the remarks, filed 10/11/2005, with respect to the USC 103 rejection over claim 17 have been fully considered and are persuasive. The rejection of claim 17 has been withdrawn. The prior does not teach or suggest the projection electrode is formed with a height such that the top end of each projection electrode is between the height of the active surface and a height of an inactive surface of the semiconductor chip.

5. Applicant's arguments regarding claims 3, 4, 6 and 26-28 have been considered but are not found persuasive. The arguments merely refer back to arguments made in previous responses. Therefore, the Examiner maintains the rejection based on the response to arguments in the action filed on 7/13/2005.

Allowable Subject Matter

6. Claims 17-20 and 29 allowed.

7. The following is an examiner's statement of reasons for allowance: The closest prior art is Skein et al and Frye et al. Sekine et al teaches forming projection electrodes, a resin sealing step,

and cutting out the semiconductor individual pieces. Frye et al teaches forming a chip-on-chip structure, but is silent to a relationship between a projection electrode height and the height of active and inactive surfaces. The prior art does not teach or suggest forming each of the projection electrodes with a height such that the top end of each projection electrode is between the height of the active surface of the semiconductor chips and the height of an inactive surface of the semiconductor chips.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takebashi et al (JP 59-092536) teaches applying a resin to a substrate and polishing (Abstract).

Olsen et al ("Calculated stresses in multilayered heteroepitaxial structures") teaches equations to determine bowing in a three layer composite, note entire reference.

9. All claims are drawn to the same invention claimed in the parent application prior to the filing of this Continued Prosecution Application under 37 CFR 1.53(d) and could have been finally rejected on the grounds and art of record in the next Office action. Accordingly, **THIS**

ACTION IS MADE FINAL even though it is a first action after the filing under 37 CFR 1.53(d). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J. Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duane Smith can be reached on 571-272-1166. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1722

MJS
December 21, 2005

ROBERT KUNEMUND
PRIMARY PATENT EXAMINER
A.U. 1722